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SE-8063

B. E. II (Sem. III) (Comp.) Examination

May / June – 2011

Computer Organization & Architecture

Time : **3** Hours] [Total Marks : **100**

Instructions :

(1)

નીચે દર્શાવેલ ☛ નિશાનીવાળી વિગતો ઉત્તરવહી પર અવશ્ય લખવી.
Fillup strictly the details of ☛ signs on your answer book.

Name of the Examination :

☛ **B. E. 2 (Sem. 3) (Comp.)**

Name of the Subject :

☛ **Computer Organization & Architecture**

☛Subject Code No. : **8 0 6 3** ☛Section No. (1, 2,.....) : **1&2**

Seat No. :

Student's Signature

1) Draw flowchart or Block diagram wherever it is necessary.

2) Make necessary assumptions if required.

SECTION - I

Q.1(a) Answer the following : 10

1. What is computer Architecture?
2. A more efficient scheme for transferring information in a system with many registers is to use a common bus system. [True / False]
3. The way the operands are chosen during program execution is dependent on the _____ of the instruction.
4. Which logical operation can be used to selectively clear particular bits of register contents?
5. What is circular shift?
6. Define: effective address.
7. What is the use of ORG instruction?
8. What is a table lookup procedure?
9. What is data linkage?
10. Define microinstruction.

(b) Attempt any two: 10

1. Explain First pass of the assembler.
2. Write an Assembly language program to add two double precision numbers.
3. What is mapping of instruction? Explain it with an example.

Q.2 Explain with diagram connection of the registers and memory of the basic computer to common bus system. 10

Or

Draw and explain flowchart for complete computer operation.

Q.3 Attempt Any Four. 20

1. Explain common bus system for four registers using multiplexers.
2. Explain 4-bit binary incrementer.
3. Discuss register transfers for the fetch phase.
4. Explain BUN and BSA with necessary micro operations.
5. Explain Decoding of micro operation fields.

SET – II (section II)

Q.4(a) Answer the following : 10

1. Enlist types of interrupts.
2. Define: hardware interlocks.
3. Give formula of speed up ratio.
4. Define: subroutine.
5. Give flynn's classification.
6. What is vector processing?

Convert the following infix statements to postfix notation.

7. (A+B)*[C*(D+E)+F]
8. (A+B) * (C/D)
9. Enlist types of CPU organization.
10. Enlist program control instructions.

(b) Attempt any Two: 10

1. A CPU has 7 registers and Common ALU with 32 operations all connected to a common bus system. Draw block diagram and formulate a control word. Show the bits of control word that specify the micro operation R6 ← R2+R3.

2. Explain Register Stack with Push and Pop Micro operations.

3. Explain four segment CPU pipeline with flowchart.

Q.5 Draw flowchart for addition and subtraction of floating point numbers and briefly explain it. 10

OR

Explain with flowchart Booth multiplication algorithm.

Q.6 Attempt Any Four. 20

1. Explain Overlapped register windows with proper diagram.

2. Enlist addressing modes and briefly explain any two with example.

3. Explain pipeline conflicts.

4. Explain SIMD array processor.

5. Explain 2-bit by 2-bit array multiplier.